

	L #	Hits	Search Text	DBs
1	L1	366	multiplier near10 alu near10 shifter	USPAT; US-PGPUB
2	L2	51	1 and sequencer	USPAT; US-PGPUB
3	L4	184	1 and (sequenc\$3 near10 instruction) not 2	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	US 20030 17224 6 A1	<input type="checkbox"/>	Circular addressing algorithms providing increased compatibility with one or more higher-level programming languages	711/220
2	US 20030 17223 8 A1	<input type="checkbox"/>	Atomically testing and setting or clearing one or more bits stored in a memory location	711/154
3	US 20030 17210 0 A1	<input type="checkbox"/>	Calculating a sum of numbers using an overflow counter in an environment exceeded by the numbers in bit-size	708/513
4	US 20030 16350 0 A1	<input type="checkbox"/>	64-bit scaled sum-of-product operations in a 32-bit environment	708/513
5	US 20030 16349 9 A1	<input type="checkbox"/>	Limiting the value of a 64-bit number to a maximum value, a minimum value, or both in a 32-bit environment	708/513
6	US 20030 14021 2 A1	<input type="checkbox"/>	Single instruction multiple data array cell	712/22
7	US 20030 12874 8 A1	<input type="checkbox"/>	Path search for CDMA implementation	375/148
8	US 20030 02884 5 A1	<input type="checkbox"/>	High performance turbo and viterbi channel decoding in digital signal processors	714/796
9	US 20030 02875 0 A1	<input type="checkbox"/>	Method and system for digital signal processing in an adaptive computing engine	712/10
10	US 20030 01468 2 A1	<input type="checkbox"/>	Clock generation systems and methods	713/500
11	US 20020 11659 5 A1	<input type="checkbox"/>	Digital signal processor integrated circuit	712/22
12	US 20020 11618 1 A1	<input type="checkbox"/>	Hardware function generator support in a DSP	704/205
13	US 20020 08934 8 A1	<input type="checkbox"/>	Programmable logic integrated circuit devices including dedicated processor components	326/38
14	US 66838 04 B1	<input type="checkbox"/>	Read/write memory arrays and methods with predetermined and retrievable latent-state patterns	365/154
15	US 65563 24 B1	<input type="checkbox"/>	Device for controlling the beam alignment in satellite laser communications systems	398/129
16	US 65105 10 B1	<input type="checkbox"/>	Digital signal processor having distributed register file	712/218
17	US 63855 45 B1	<input type="checkbox"/>	Method and apparatus for determining dip angle and horizontal and vertical conductivities	702/10
18	US 63321 88 B1	<input type="checkbox"/>	Digital signal processor with bit FIFO	712/204
19	US 63178 19 B1	<input type="checkbox"/>	Digital signal processor containing scalar processor and a plurality of vector processors operating from a single instruction	712/22

	Docum ent ID	U	Title	Current OR
20	US 62302 78 B1	<input type="checkbox"/>	Microprocessor with functional units that can be selectively coupled	713/324
21	US 62188 41 B1	<input type="checkbox"/>	Method and apparatus for determining dip angle, and horizontal and vertical conductivities using multi frequency measurments and a model	324/338
22	US 61638 36 A	<input type="checkbox"/>	Processor with programmable addressing modes	712/37
23	US 61122 98 A	<input type="checkbox"/>	Method for managing an instruction execution pipeline during debugging of a data processing system	712/227
24	US 60947 26 A	<input type="checkbox"/>	Digital signal processor using a reconfigurable array of macrocells	713/400
25	US 60920 24 A	<input type="checkbox"/>	Method and apparatus for determining resistivity and dielectric anisotropy parameters of earth formations by using multifrequency and/or multispacing measurements	702/7
26	US 60818 85 A	<input type="checkbox"/>	Method and apparatus for halting a processor and providing state visibility on a pipeline phase basis	712/227
27	US 60651 06 A	<input type="checkbox"/>	Resuming normal execution by restoring without refetching instructions in multi-word instruction register interrupted by debug instructions loading and processing	712/24
28	US 60617 79 A	<input type="checkbox"/>	Digital signal processor having data alignment buffer for performing unaligned data accesses	712/204
29	US 60556 49 A	<input type="checkbox"/>	Processor test port with scan chains and data streaming	714/30
30	US 60165 55 A	<input type="checkbox"/>	Non-intrusive software breakpoints in a processor instruction execution pipeline	714/35
31	US 59702 41 A	<input type="checkbox"/>	Maintaining synchronism between a processor pipeline and subsystem pipelines during debugging of a data processing system	712/227
32	US 59548 11 A	<input type="checkbox"/>	Digital signal processor architecture	712/35
33	US 59266 44 A	<input type="checkbox"/>	Instruction formats/instruction encoding	712/22
34	US 58965 43 A	<input type="checkbox"/>	Digital signal processor architecture	712/35
35	US 58699 68 A	<input type="checkbox"/>	Method and apparatus for avoiding mutual coupling between receivers in measurement while drilling	324/338
36	US 58119 72 A	<input type="checkbox"/>	Method and apparatus for determining influence of mutual magnetic coupling in electromagnetic propagation tools	324/338
37	US 57520 68 A	<input type="checkbox"/>	Mesh parallel computer architecture apparatus and associated methods	712/16
38	US 57178 91 A	<input type="checkbox"/>	Digital signal processor with caching of instructions that produce a memory conflict	711/125
39	US 56850 05 A	<input type="checkbox"/>	Digital signal processor configured for multiprocessing	712/36
40	US 56820 99 A	<input type="checkbox"/>	Method and apparatus for signal bandpass sampling in measurement-while-drilling applications	324/338
41	US 56340 76 A	<input type="checkbox"/>	DMA controller responsive to transition of a request signal between first state and second state and maintaining of second state for controlling data transfer	710/22
42	US 56197 20 A	<input type="checkbox"/>	Digital signal processor having link ports for point-to-point communication	712/38

	Docum ent ID	U	Title	Current OR
43	US 56170 58 A	<input type="checkbox"/>	Digital signal processing for linearization of small input signals to a tri-state power switch	330/10
44	US 56110 75 A	<input type="checkbox"/>	Bus architecture for digital signal processor allowing time multiplexed access to memory banks	711/153
45	US 55903 56 A	<input type="checkbox"/>	Mesh parallel computer architecture apparatus and associated methods	712/31
46	US 55743 74 A	<input type="checkbox"/>	Method and apparatus for interrogating a borehole and surrounding formation utilizing digitally controlled oscillators	324/338
47	US 53793 88 A	<input type="checkbox"/>	Digital signal processing apparatus with sequencer designating program routines	712/248
48	US 53654 65 A	<input type="checkbox"/>	Floating point to logarithm converter	708/204
49	US 52336 98 A	<input type="checkbox"/>	Method for operating data processors	713/601
50	US 51558 17 A	<input type="checkbox"/>	Microprocessor	712/218
51	US 50620 41 A	<input type="checkbox"/>	Processor/coprocessor interface apparatus including microinstruction clock synchronization	712/221

	Docum ent ID	U	Title	Current OR
1	US 20040 03995 2 A1	<input type="checkbox"/>	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/300
2	US 20040 03990 0 A1	<input checked="" type="checkbox"/>	Processor, program conversion apparatus, program conversion method, and computer program	712/234
3	US 20040 01568 0 A1	<input checked="" type="checkbox"/>	Data processor for modifying and executing operation of instruction code	712/226
4	US 20040 01032 1 A1	<input checked="" type="checkbox"/>	Data processor and program	700/2
5	US 20030 22600 2 A1	<input checked="" type="checkbox"/>	Devices, systems and methods for conditional instructions notice	712/234
6	US 20030 20042 3 A1	<input checked="" type="checkbox"/>	Repeat block with zero cycle overhead nesting	712/228
7	US 20030 19607 2 A1	<input checked="" type="checkbox"/>	Digital signal processor architecture for high computation speed	712/32
8	US 20030 19605 8 A1	<input checked="" type="checkbox"/>	Memory system for supporting multiple parallel accesses at very high frequencies	711/169
9	US 20030 16367 9 A1	<input checked="" type="checkbox"/>	Method and apparatus for loop buffering digital signal processing instructions	712/241
10	US 20030 05613 4 A1	<input checked="" type="checkbox"/>	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/324
11	US 20030 05608 8 A1	<input checked="" type="checkbox"/>	Processor, compiler and compilation method	712/214
12	US 20030 02383 3 A1	<input checked="" type="checkbox"/>	Apparatus and systems for dyadic digital signal processing instructions	712/35
13	US 20030 02383 2 A1	<input checked="" type="checkbox"/>	Instruction set architecture for signal processors	712/35
14	US 20030 01888 2 A1	<input checked="" type="checkbox"/>	Dyadic DSP instructions for digital signal processors	712/35
15	US 20030 01888 1 A1	<input checked="" type="checkbox"/>	Methods of dyadic DSP instruction operation	712/35
16	US 20020 18882 4 A1	<input checked="" type="checkbox"/>	Method and apparatus for instruction set architecture to perform primary and shadow digital signal processing sub-instructions simultaneously	712/35
17	US 20020 18447 2 A1	<input checked="" type="checkbox"/>	Microcomputer	712/33

	Docum ent ID	U	Title	Current OR
18	US 20020 17834 7 A1	<input checked="" type="checkbox"/>	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
19	US 20020 13871 5 A1	<input checked="" type="checkbox"/>	Microprocessor executing data transfer between memory and register and data transfer between registers in response to single push/pop instruction	712/225
20	US 20020 12083 0 A1	<input checked="" type="checkbox"/>	Data processor assigning the same operation code to multiple operations	712/209
21	US 20020 11618 6 A1	<input checked="" type="checkbox"/>	Voice activity detector for integrated telecommunications processing	704/233
22	US 20020 11214 4 A1	<input checked="" type="checkbox"/>	APPARATUS AND METHOD FOR CODE-ENHANCED PERFORMANCE IN A DIGITAL SIGNAL PROCESSING UNIT	712/29
23	US 20020 07603 4 A1	<input checked="" type="checkbox"/>	Tone detection for integrated telecommunications processing	379/390 .02
24	US 20020 06413 9 A1	<input checked="" type="checkbox"/>	Network echo canceller for integrated telecommunications processing	370/289
25	US 20020 04162 6 A1	<input checked="" type="checkbox"/>	Media processing apparatus which operates at high efficiency	375/240
26	US 20020 02654 5 A1	<input checked="" type="checkbox"/>	Data processing apparatus of high speed process using memory of low speed and low power consumption	710/56
27	US 20020 00267 0 A1	<input checked="" type="checkbox"/>	DATA PROCESSING DEVICE	712/245
28	US 20010 01007 2 A1	<input checked="" type="checkbox"/>	Instruction translator translating non-native instructions for a processor into native instructions therefor, instruction memory with such translator, and data processing apparatus using them	712/209
29	US 66717 97 B1	<input checked="" type="checkbox"/>	Microprocessor with expand instruction for forming a mask from one bit	712/224
30	US 66585 78 B1	<input checked="" type="checkbox"/>	Microprocessors	713/324
31	US 66437 68 B2	<input checked="" type="checkbox"/>	Dyadic DSP instruction processor with main and sub-operation functional blocks selected from each set of multiplier and adder	712/221
32	US 66314 61 B2	<input checked="" type="checkbox"/>	Dyadic DSP instructions for digital signal processors	712/221
33	US 66153 39 B1	<input checked="" type="checkbox"/>	VLIW processor accepting branching to any instruction in an instruction word set to be executed consecutively	712/24
34	US 65981 55 B1	<input checked="" type="checkbox"/>	Method and apparatus for loop buffering digital signal processing instructions	712/241
35	US 65947 28 B1	<input checked="" type="checkbox"/>	Cache memory with dual-way arrays and multiplexed parallel output	711/127
36	US 65747 24 B1	<input checked="" type="checkbox"/>	Microprocessor with non-aligned scaled and unscaled addressing	711/220

	Docum ent ID	U	Title	Current OR
37	US 65679 10 B2	<input checked="" type="checkbox"/>	Digital signal processing unit with emulation circuitry and debug interrupt enable register indicating serviceable time-critical interrupts during real-time emulation mode	712/227
38	US 65500 00 B1	<input checked="" type="checkbox"/>	Processor to execute in parallel plurality of instructions using plurality of functional units, and instruction allocation controller	712/215
39	US 65394 67 B1	<input checked="" type="checkbox"/>	Microprocessor with non-aligned memory access	711/219
40	US 64703 76 B1	<input checked="" type="checkbox"/>	Processor capable of efficiently executing many asynchronous event tasks	718/108
41	US 64635 20 B1	<input checked="" type="checkbox"/>	Processor for executing instruction codes of two different lengths and device for inputting the instruction codes	712/205
42	US 64461 95 B1	<input checked="" type="checkbox"/>	Dyadic operations instruction processor with configurable functional blocks	712/221
43	US 64346 90 B1	<input checked="" type="checkbox"/>	Microprocessor having a DSP and a CPU and a decoder discriminating between DSP-type instructions and CUP-type instructions	712/35
44	US 64120 64 B1	<input checked="" type="checkbox"/>	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
45	US 64083 76 B1	<input checked="" type="checkbox"/>	Method and apparatus for instruction set architecture to perform primary and shadow digital signal processing sub-instructions simultaneously	712/36
46	US 64053 02 B1	<input checked="" type="checkbox"/>	Microcomputer	712/35
47	US 63743 46 B1	<input checked="" type="checkbox"/>	Processor with conditional execution of every instruction	712/221
48	US 63413 24 B1	<input checked="" type="checkbox"/>	Exception processing in superscalar microprocessor	710/260
49	US 63341 81 B1	<input checked="" type="checkbox"/>	DSP with wait state registers having at least two portions	712/38
50	US 63276 31 B1	<input checked="" type="checkbox"/>	Signal processing apparatus	709/400
51	US 63246 39 B1	<input checked="" type="checkbox"/>	Instruction converting apparatus using parallel execution code	712/212
52	US 63112 64 B1	<input checked="" type="checkbox"/>	Digital signal processor with wait state register	712/38
53	US 63109 21 B1	<input checked="" type="checkbox"/>	Media processing apparatus which operates at high efficiency	375/240 .26
54	US 63016 55 B1	<input checked="" type="checkbox"/>	Exception processing in asynchronous processor	712/244
55	US 62928 81 B1	<input checked="" type="checkbox"/>	Microprocessor, operation process execution method and recording medium	712/41
56	US 62827 08 B1	<input checked="" type="checkbox"/>	Method and processor for structuring a multi-instruction computer program in an internal directed acyclic graph	717/156
57	US 62667 55 B1	<input checked="" type="checkbox"/>	Translation lookaside buffer with virtual address conflict prevention	711/210
58	US 62634 19 B1	<input checked="" type="checkbox"/>	Integrated circuit with wait state registers	712/38
59	US 62634 18 B1	<input checked="" type="checkbox"/>	Process of operating a microprocessor to use wait state numbers	712/38

	Docum ent ID	U	Title	Current OR
60	US 62600 88 B1	<input checked="" type="checkbox"/>	Single integrated circuit embodying a risc processor and a digital signal processor	710/100
61	US 62533 07 B1	<input checked="" type="checkbox"/>	Data processing device with mask and status bits for selecting a set of status conditions	712/209
62	US 62498 60 B1	<input checked="" type="checkbox"/>	System with wait state registers	712/38
63	US 62471 11 B1	<input checked="" type="checkbox"/>	System with wait state register	712/38
64	US 62438 01 B1	<input checked="" type="checkbox"/>	System with wait state registers	712/38
65	US 62437 35 B1	<input checked="" type="checkbox"/>	Microcontroller, data processing system and task switching control method	718/102
66	US 62405 05 B1	<input checked="" type="checkbox"/>	System with wait state registers	712/38
67	US 62405 04 B1	<input checked="" type="checkbox"/>	Process of operating a microprocessor to change wait states	712/38
68	US 62162 00 B1	<input checked="" type="checkbox"/>	Address queue	711/100
69	US 62090 79 B1	<input checked="" type="checkbox"/>	Processor for executing instruction codes of two different lengths and device for inputting the instruction codes	712/210
70	US 61784 92 B1	<input checked="" type="checkbox"/>	Data processor capable of executing two instructions having operand interference at high speed in parallel	712/23
71	US 61675 09 A	<input checked="" type="checkbox"/>	Branch performance in high speed processor	712/237
72	US 61345 78 A	<input checked="" type="checkbox"/>	Data processing device and method of operation with context switching	718/100
73	US 61311 57 A	<input checked="" type="checkbox"/>	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
74	US 61287 25 A	<input checked="" type="checkbox"/>	Microprocessor with an instruction for setting or clearing a bit field	712/200
75	US 61287 24 A	<input checked="" type="checkbox"/>	Computation using codes for controlling configurable computational circuit	712/32
76	US 61122 89 A	<input checked="" type="checkbox"/>	Data processor	712/23
77	US 61087 65 A	<input checked="" type="checkbox"/>	Device for digital signal processing	712/32
78	US 60921 84 A	<input checked="" type="checkbox"/>	Parallel processing of pipelined instructions having register dependencies	712/218
79	US 60761 58 A	<input checked="" type="checkbox"/>	Branch prediction in high-performance processor	712/230
80	US 60700 03 A	<input checked="" type="checkbox"/>	System and method of memory access in apparatus having plural processors and plural memories	710/317
81	US 60556 28 A	<input checked="" type="checkbox"/>	Microprocessor with a nestable delayed branch instruction without branch related pipeline interlocks	712/235
82	US 60385 84 A	<input checked="" type="checkbox"/>	Synchronized MIMD multi-processing system and method of operation	709/248

	Docum ent ID	U	Title	Current OR
83	US 60212 65 A	<input checked="" type="checkbox"/>	Interoperability with multiple instruction sets	712/209
84	US 60031 29 A	<input checked="" type="checkbox"/>	System and method for handling interrupt and exception events in an asymmetric multiprocessor architecture	712/244
85	US 60000 25 A	<input checked="" type="checkbox"/>	Method of signal processing by contemporaneous operation of ALU and transfer of data	712/32
86	US 59960 58 A	<input checked="" type="checkbox"/>	System and method for handling software interrupts with argument passing	712/31
87	US 59957 46 A	<input checked="" type="checkbox"/>	Byte-compare operation for high-performance processor	712/220
88	US 59602 09 A	<input checked="" type="checkbox"/>	Scaleable digital signal processor with parallel architecture	712/1
89	US 59464 83 A	<input checked="" type="checkbox"/>	Devices, systems and methods for conditional instructions	712/223
90	US 59336 24 A	<input checked="" type="checkbox"/>	Synchronized MIMD multi-processing system and method inhibiting instruction fetch at other processors while one processor services an interrupt	709/400
91	US 59077 14 A	<input checked="" type="checkbox"/>	Method for pipelined data processing with conditioning instructions for controlling execution of instructions without pipeline flushing	712/23
92	US 58988 78 A	<input checked="" type="checkbox"/>	Data processing system having capability to interpolate processing coefficients	710/260
93	US 58929 38 A	<input checked="" type="checkbox"/>	Interactive interface system	710/8
94	US 58812 72 A	<input checked="" type="checkbox"/>	Synchronized MIMD multi-processing system and method inhibiting instruction fetch at other processors on write to program counter of one processor	709/400
95	US 58810 77 A	<input checked="" type="checkbox"/>	Data processing system	714/800
96	US 58677 26 A	<input checked="" type="checkbox"/>	Microcomputer	712/32
97	US 58549 07 A	<input checked="" type="checkbox"/>	Microcomputer for digital signal processing having on-chip memory and external memory access	710/100
98	US 58290 54 A	<input checked="" type="checkbox"/>	Devices and systems with parallel logic unit operable on data memory locations	711/202
99	US 58288 96 A	<input checked="" type="checkbox"/>	Microcomputer system for digital signal processing	712/33
100	US 58285 77 A	<input checked="" type="checkbox"/>	Devices and systems with protective terminal configuration, and methods	716/4
101	US 58261 11 A	<input checked="" type="checkbox"/>	Modem employing digital signal processor	710/69
102	US 58260 55 A	<input checked="" type="checkbox"/>	System and method for retiring instructions in a superscalar microprocessor	712/218
103	US 58092 88 A	<input checked="" type="checkbox"/>	Synchronized MIMD multi-processing system and method inhibiting instruction fetch on memory access stall	709/400
104	US 58023 85 A	<input checked="" type="checkbox"/>	Array processing system with each processor including router and which selectively delays input/output of individual processors in response delay instructions	712/16
105	US 57784 23 A	<input checked="" type="checkbox"/>	Prefetch instruction for improving performance in reduced instruction set processor	711/118

	Docum ent ID	U	Title	Current OR
106	US 57778 85 A	<input checked="" type="checkbox"/>	Devices and systems with protective terminal configuration, and methods	716/1
107	US 57686 09 A	<input checked="" type="checkbox"/>	Reduced area of crossbar and method of operation	712/11
108	US 57652 19 A	<input checked="" type="checkbox"/>	Apparatus and method for incrementally accessing a system memory	711/220
109	US 57650 13 A	<input checked="" type="checkbox"/>	Digital signal processor	712/17
110	US 57649 43 A	<input checked="" type="checkbox"/>	Data path circuitry for processor having multiple instruction pipelines	712/218
111	US 57581 95 A	<input checked="" type="checkbox"/>	Register to memory data transfers with field extraction and zero/sign extension based upon size and mode data corresponding to employed address register	712/300
112	US 57581 15 A	<input checked="" type="checkbox"/>	Interoperability with multiple instruction sets	712/209
113	US 57581 12 A	<input checked="" type="checkbox"/>	Pipeline processor with enhanced method and apparatus for restoring register-renaming information in the event of a branch misprediction	712/217
114	US 57520 73 A	<input checked="" type="checkbox"/>	Digital signal processor architecture	712/35
115	US 57427 80 A	<input checked="" type="checkbox"/>	Dual pipeline superscalar reduced instruction set computer system architecture	712/206
116	US 57404 49 A	<input checked="" type="checkbox"/>	Method and apparatus for managing interrupts in a data processing system	710/260
117	US 57242 48 A	<input checked="" type="checkbox"/>	Devices and systems with protective terminal configuration, and methods	716/4
118	US 57179 46 A	<input checked="" type="checkbox"/>	Data processor	712/225
119	US 56969 13 A	<input checked="" type="checkbox"/>	Unique processor identifier in a multi-processing system having plural memories with a unified address space corresponding to each processor	710/317
120	US 56844 35 A	<input checked="" type="checkbox"/>	Analog waveform communications reduced instruction set processor	332/117
121	US 56529 10 A	<input checked="" type="checkbox"/>	Devices and systems with conditional instructions	712/218
122	US 56258 38 A	<input checked="" type="checkbox"/>	Microcomputer system for digital signal processing	712/32
123	US 56175 74 A	<input checked="" type="checkbox"/>	Devices, systems and methods for conditional instructions	712/200
124	US 56153 83 A	<input checked="" type="checkbox"/>	Microcomputer system for digital signal processing	712/43
125	US 56131 46 A	<input checked="" type="checkbox"/>	Reconfigurable SIMD/MIMD processor using switch matrix to allow access to a parameter memory by any of the plurality of processors	712/20
126	US 56065 20 A	<input checked="" type="checkbox"/>	Address generator with controllable modulo power of two addressing capability	708/491
127	US 56030 47 A	<input checked="" type="checkbox"/>	Superscalar microprocessor architecture	712/23
128	US 55924 05 A	<input checked="" type="checkbox"/>	Multiple operations employing divided arithmetic logic unit and multiple flags register	708/518

	Docum ent ID	U	Title	Current OR
129	US 55862 75 A	<input checked="" type="checkbox"/>	Devices and systems with parallel logic unit operable on data memory locations, and methods	712/223
130	US 55837 67 A	<input checked="" type="checkbox"/>	Devices and systems with parallel logic unit, and methods notice	701/1
131	US 55817 92 A	<input checked="" type="checkbox"/>	Microcomputer system for digital signal processing having external peripheral and memory access	710/52
132	US 55794 97 A	<input checked="" type="checkbox"/>	Devices and systems with parallel logic unit, and methods	375/222
133	US 55792 18 A	<input checked="" type="checkbox"/>	Devices and systems with parallel logic unit, and methods	700/1
134	US 55686 24 A	<input checked="" type="checkbox"/>	Byte-compare operation for high-performance processor	712/223
135	US 55509 93 A	<input checked="" type="checkbox"/>	Data processor with sets of two registers where both registers receive identical information and when context changes in one register the other register remains unchanged	712/229
136	US 55220 83 A	<input checked="" type="checkbox"/>	Reconfigurable multi-processor operating in SIMD mode with one processor fetching instructions for use by remaining processors	712/22
137	US 55174 36 A	<input checked="" type="checkbox"/>	Digital signal processor for audio applications	708/524
138	US 54715 92 A	<input checked="" type="checkbox"/>	Multi-processor with crossbar link of processors and memories and method of operation	709/213
139	US 54695 51 A	<input checked="" type="checkbox"/>	Method and apparatus for eliminating branches using conditional move instructions	712/239
140	US 54540 91 A	<input checked="" type="checkbox"/>	Virtual to physical address translation scheme with granularity hint for identifying subsequent pages to be accessed	711/203
141	US 54505 53 A	<input checked="" type="checkbox"/>	Digital signal processor including address generation by execute/stop instruction designated	711/214
142	US 54106 82 A	<input checked="" type="checkbox"/>	In-register data manipulation for unaligned byte write using data shift in reduced instruction set processor	712/300
143	US 54106 49 A	<input checked="" type="checkbox"/>	Imaging computer system and network	345/505
144	US 53718 96 A	<input checked="" type="checkbox"/>	Multi-processor having control over synchronization of processors in mind mode and method of operation	712/20
145	US 53677 05 A	<input checked="" type="checkbox"/>	In-register data manipulation using data shift in reduced instruction set processor	712/41
146	US 53496 87 A	<input checked="" type="checkbox"/>	Speech recognition system having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	704/231
147	US 53394 47 A	<input checked="" type="checkbox"/>	Ones counting circuit, utilizing a matrix of interconnected half-adders, for counting the number of ones in a binary string of image data	377/82
148	US 53197 92 A	<input checked="" type="checkbox"/>	Modem having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228
149	US 53197 89 A	<input checked="" type="checkbox"/>	Electromechanical apparatus having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228
150	US 53136 48 A	<input checked="" type="checkbox"/>	Signal processing apparatus having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228

	Docum ent ID	U	Title	Current OR
151	US 52414 92 A	<input checked="" type="checkbox"/>	Apparatus for performing multiply and accumulate instructions with reduced power and a method therefor	708/523
152	US 52396 54 A	<input checked="" type="checkbox"/>	Dual mode SIMD/MIMD processor providing reuse of MIMD instruction memories as data memories when operating in SIMD mode	712/20
153	US 52333 35 A	<input checked="" type="checkbox"/>	Symbol/raster generator for CRT display	345/17
154	US 52261 25 A	<input checked="" type="checkbox"/>	Switch matrix having integrated crosspoint logic and method of operation	710/317
155	US 52187 10 A	<input checked="" type="checkbox"/>	Audio signal processing system having independent and distinct data buses for concurrently transferring audio signal data to provide acoustic control	704/278
156	US 52127 77 A	<input checked="" type="checkbox"/>	Multi-processor reconfigurable in single instruction multiple data (SIMD) and multiple instruction multiple data (MIMD) modes and method of operation	712/229
157	US 51971 40 A	<input checked="" type="checkbox"/>	Sliced addressing multi-processor and method of operation	711/220
158	US 51931 67 A	<input checked="" type="checkbox"/>	Ensuring data integrity by locked-load and conditional-store operations in a multiprocessor system	711/163
159	US 51558 12 A	<input checked="" type="checkbox"/>	Devices and method for generating and using systems, software waitstates on address boundaries in data processing	710/59
160	US 51426 77 A	<input checked="" type="checkbox"/>	Context switching devices, systems and methods	718/108
161	US 51366 64 A	<input checked="" type="checkbox"/>	Pixel rendering	382/304
162	US 51288 90 A	<input checked="" type="checkbox"/>	Apparatus for performing multiplications with reduced power and a method therefor	708/625
163	US 50724 18 A	<input checked="" type="checkbox"/>	Series maximum/minimum function computing devices, systems and methods	708/207
164	US 50654 33 A	<input checked="" type="checkbox"/>	Audio signal data processing system	381/63
165	US 47137 49 A	<input checked="" type="checkbox"/>	Microprocessor with repeat instruction	712/241
166	US 47137 48 A	<input checked="" type="checkbox"/>	Microprocessor with block move instruction	712/225
167	US 46775 86 A	<input checked="" type="checkbox"/>	Microcomputer device having test mode substituting external RAM for internal RAM	714/27
168	US 46384 51 A	<input checked="" type="checkbox"/>	Microprocessor system with programmable interface	710/69
169	US 46086 34 A	<input checked="" type="checkbox"/>	Microcomputer with offset in store-accumulator operations	712/221
170	US 45861 31 A	<input checked="" type="checkbox"/>	Microcomputer having data move circuits for within-memory shift of data words	712/221
171	US 45772 82 A	<input checked="" type="checkbox"/>	Microcomputer system for digital signal processing	712/33
172	US 45582 32 A	<input checked="" type="checkbox"/>	Level detector circuit for microcomputer devices	327/78
173	US 45382 39 A	<input checked="" type="checkbox"/>	High-speed multiplier for microcomputer used in digital signal processing system	708/627

	Docum ent ID	U	Title	Current OR
174	US 45339 92 A	<input checked="" type="checkbox"/>	Microcomputer having shifter in ALU input	712/42
175	US 45286 25 A	<input checked="" type="checkbox"/>	Input/output instruction execution in microcomputer	712/225
176	US 45190 31 A	<input checked="" type="checkbox"/>	Microcomputer with accumulator saturation upon overflow	712/32
177	US 45148 05 A	<input checked="" type="checkbox"/>	Interrupt operation in systems emulator mode for microcomputer	710/261
178	US 45148 01 A	<input checked="" type="checkbox"/>	Microcomputer with table-read and table-write instructions	712/205
179	US 45077 27 A	<input checked="" type="checkbox"/>	Microcomputer with ROM test mode of operation	712/33
180	US 45063 22 A	<input checked="" type="checkbox"/>	Read/write memory cell for microcomputer	711/169
181	US 45035 00 A	<input checked="" type="checkbox"/>	Microcomputer with bus interchange module	712/33
182	US 44981 35 A	<input checked="" type="checkbox"/>	Microcomputer with accumulator addressing	712/33
183	US 44941 87 A	<input checked="" type="checkbox"/>	Microcomputer with high speed program memory	712/37
184	US 44919 10 A	<input type="checkbox"/>	Microcomputer having data shift within memory	712/42